ABSTRACT OF THE DISCLOSURE

A network switch having an internet port interface controller, includes a high performance interface for communicating with other switches and components through the transfer of data packets contained in memory. The high performance interface includes a data connection bus, where data is transferred on both a rising edge and a falling edge of a clock signal, and the data connection bus has output drivers and a multiplexing circuit connected to the output drivers. The multiplexing circuit is constructed through two levels of glitchless multiplexors, to serialize said data transmitted over said high performance interface. Because two levels of glitchless multiplexors are employed, function hazards that occur in the glitchless multiplexors when more than one input thereto change simultaneously can be masked, and do not create noise that can be propagated to an output driver.